DESCRIPTION AMENDMENTS

**Rewrite paragraph [0001] to read as follows:**

This application has subject matter in common with ~~U.S. Patent Application No. _____ (attorney docket number FORT 2769)~~ U.S. Patent Application No. 10/735,342 entitled RESOURCE BOARD FOR EMULATION SYSTEM filed concurrently herewith.

**Rewrite paragraph [0053] to read as follows:**

FIG. 15 is a block diagram of a circuit board 70 implementing emulation system 69 of FIG. 14. ~~U.S. Patent Application No. _____ (attorney docket number FORT 2769)~~ U.S. Patent Publication 2004/0254906 entitled RESOURCE BOARD FOR EMULATION SYSTEM ~~filed concurrently herewith and incorporated herein by reference,~~ based on U.S. Patent Application No. 10/735,342 filed December 11, 2003, and incorporated herein by reference, describes circuit board 70 in detail. A set of field programmable gate arrays (FPGAs) 72 for emulating IC logic reside on circuit board 70, and conductors (not shown) interconnect some of the input/output (IO) terminals of each FPGA 72 to IO terminals of each of the other FPGAs 72. An interface circuit 38 provides external equipment with access to other IO terminals and to programming terminals of each FPGA 72. A clock source 74 supplies a set of clock signals of various frequencies to another FPGA 76 programmed to generate both primary and secondary clock signals for the emulated IC using the clock signals from clock source 74 as timing references. FPGA 76 may also use clock ~~signal~~ signals generated by equipment external to circuit board 70 as timing references.